IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Kamilo Feher

Serial No. *to be assigned*
Filing Date: herewith

For:

Feher Keying (FK) Modulation And Transceivers Including Clock Shaping Processors

Attorney Docket No. A-66944-1/RMA

December 7, 2000

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicant respectfully requests the following preliminary amendments be entered:

IN THE SPECIFICATION

Page 1:10: insert in the blank after "Serial No." –09/370,361—.

Page 2:3: insert in the blank after "Serial No." –09/370,362—.

IN THE CLAIMS

1. (Amended) A structure comprising:

a shaped clock signal generator receiving a data signal having a data bit rate and generating a shaped data information bearing clock signal, said shaped clock signal generator being synchronous or asynchronous with the data bit rate of the received data signal; and

a data signal processor having a receiver port and a control signal generation means for selecting the shaped data information bearing clock signal for further transmission and/or modulation.

Cancel Claims 2-3 without prejudice.

4. (Amended) A structure comprising:

a clock generator [which provides] communicating clock signals to [two or more] a plurality of data information bearing clock transition time-shifting and clock-shaping signal generators;

[a data input port and connection to] a data interface input encoder [for the generation of] providing a clock selector data signal [by said data input interface encoder]; and

a switch [to choose,] receiving said clock selector data signal and selecting, based on said clock selector data signal, one of the clock transition time-shifted shaped data information bearing clock signals and connecting the selected signal to [the] a data interface output unit; [and]

said [a] data interface output unit [for connecting] coupling the selected signal to [the] a signal transmission medium or to further signal processing.

5. (Amended) A transmit signal processor structure comprising:

a first clock signal generator having a first set of clock shaping data information bearing parameters and generating a first clock shaped signal;

a second clock signal generator having a second set of clock shaping data information bearing parameters and generating a second clock shaped signal, said second set of clock shaping parameters having at least one parameter different from that of the first set of clock signal shaping parameters;

a data input receive [circuitry and processor for selection] circuit selecting of one of the said first or second clock shaped signals;

[a switch for switching between the first set and second set of shaped clock parameters; and]

a switch selecting between the first clock shaped signal and the second clock shaped signal; and

an output interface [port to provide] communicating the selected signal to the transmission medium.

6. (Amended) A spectral saving data and clock signal processing system comprising:

a data signal and clock signal [processing means to provide] processor providing a clock modulated data information bearing signal having changeable [distances] time duration between the rising edges and falling edges of the modulated data information bearing clock signals; [and]

a control [means] unit having its input connected to the data signal source and its output connected to edge distance switch selection means; and

a digital interface output [means to] circuit connecting the clock modulated data information bearing signal to [the] an input interface of [the] a subsequent signal processor.

7. (Amended) A clock signal modulator comprising:

a data input interface [means to provide] providing data signals to an external asynchronous pure clock source; and

[an asynchronous pure clock generator means to provide a pure clock signal; and]

a selector switch means which is controlled by the data input interface [means to provide a] selecting a data information bearing clock modulated signal having a shorter temporal distance between the falling edge and rising edge of the clock modulated signal for a zero state data signal and a longer temporal distance between the falling edge and rising edge of the clock modulated signal for a one-state data signal, said shorter temporal distance and said longer temporal distance encoding said data information into said clock modulated signal.

8. (Amended) A clock converter system [comprised of] comprising:

an input data interface [means for] coupled to a clock signal selection means for controlling the selection [process of the] of an output shaped clock signal [which is provided to the an interface output unit means];

[a] clock signal shaping means [to provide] providing smoothed continuous data information bearing clock signals to the clock signal selection means, said clock signal shaping means having one or more different clock signal data information bearing parameters used to provide different; and

an output signal [processing means to] processor accepting the smoothed different clock signal data information bearing parameter processed clock converted signals.

9. (Amended) A clock modulated signaling system comprising:

an input data interface [means] to provide control signal generation and selection [means] of shaped data information bearing clock signals;

an interface [means] to provide signal processing [means for] to modulate[ing] the clock modulated baseband signal [by means of] using a cross-correlated quadrature modulator system;

an output amplifier [means] receiving the cross-correlated quadrature modulated signal and generating an amplified [to connect the] cross-correlated quadrature modulated signal for transmission to a [the] transmission medium;

a demodulator [demodulation means to demodulate the received] receiving and demodulating the amplified cross-correlated quadrature modulated signal; and

signal processor means to decode and regenerate the data information bearing clock modulated signal from the received and demodulated signal.

Cancel Claim 10 without prejudice.

11. (Amended) A method comprising steps:

receiving a data signal;

generating a shaped data information bearing clock signal in response to said received data signal;

generating a control signal for selecting said generated shaped data information bearing clock signal; and

processing said selected shaped data information bearing clock signal for transmission or modulation.

12. (Amended) The method in Claim 11, wherein said shaped data information bearing clock signal is generated synchronously with a data bit rate of said received data signal.

13. (Amended) The method in Claim 11, wherein said shaped data information bearing clock signal is generated asynchronously with a data bit rate of said received data signal.

14. (Amended) A method of signaling using clock modulated signals, said method comprising:

selecting at least one shaped data information bearing clock signal;

cross-correlating and quadrature modulating said at least one selected [at least one] shaped data information bearing clock signal;

amplifying said cross-correlated quadrature modulated shaped data information bearing clock signal;

transmitting said amplified cross-correlated quadrature modulated shaped data information bearing clock signal;

receiving said transmitted amplified cross-correlated quadrature modulated shaped data information bearing clock signal;

demodulating said received shaped data information bearing clock signal; and

decoding said received demodulated shaped data information bearing clock signal and regenerating said selected shaped data information bearing clock signal.

15. (Amended) The method of signaling in claim 14, wherein said shaped data information bearing clock signals are selected from the group consisting of: shaped symmetrical data information bearing clock signals, shaped non-symmetrical data information bearing clock signals, two-level non-symmetrical data information bearing clock signals, multilevel non-symmetrical data information bearing clock signals, variable rise and different non-symmetrical fall time data information bearing clock signals, asynchronous data information bearing clock signal information, and combinations thereof.

16. (Amended) The method of signaling in claim 14, wherein said shaped data information bearing clock signals include clock signals having sinusoidal and square wave components.

17. (Amended) The method of signaling in claim 14, wherein said shaped data information bearing clock signals include clock signals having at least one first shaped clock having a longer duration

relative to a second shaped clock and said second shaped clock having a shorter duration relative to said first shaped clock.

18. (Amended) The method of signaling in claim 14, wherein said shaped data information bearing clock signals include clock signals having at least one shaped data information bearing clock having a rounded-off longer duration and a second shaped clock having a shaped rounded-off shorter duration.

19. (Amended) The method of signaling in claim 14, wherein said shaped data information bearing clock signals include clock signals having variable amplitude clock levels, and wherein a first clock level is used for a 1 logical state and a second clock level is used for a 0 logical state of quadrature I and Q signal patterns.

20. (Amended) The method of signaling in claim 14, wherein said shaped data information bearing clock signals include clock signals having a longer than 50% high state duration for the one state data and a shorter than 50% high state duration for the zero state data.

21. (Amended) A system comprising:

a shaped clock signal generator receiving a data signal having a data bit rate and generating a shaped data information bearing clock signal, said shaped clock signal generator being either synchronous or asynchronous with the data bit rate of the received data signal; and

a data signal processor having a receiver port and a control signal generation circuit for selecting said shaped data information bearing clock signal.

22. (Unchanged) The system in claim 21, wherein said shaped clock signals are selected from the group consisting of: shaped symmetrical clock signals, shaped non-symmetrical clock signals, two-level non-symmetrical clock signals, multilevel non-symmetrical clock signals, variable rise and different non-symmetrical fall time clock signals, asynchronous clock signal information, and combinations thereof.

23. (Unchanged) The system in claim 21, wherein said shaped clock signals include clock signals having sinusoidal and square wave components.

24. (Unchanged) The system in claim 21, wherein said shaped clock signals include clock signals having at least one first shaped clock having a longer duration relative to a second shaped clock and said second shaped clock having a shorter duration relative to said first shaped clock.

25. (Unchanged) The system in claim 21, wherein said shaped clock signals include clock signals having at least one shaped clock having a rounded-off longer duration and a second shaped clock having a shaped rounded-off shorter duration.

26. (Unchanged) The system in claim 21, wherein said shaped clock signals include clock signals having variable amplitude clock levels, and wherein a first clock level is used for a 1 logical state and a second clock level is used for a 0 logical state of quadrature I and Q signal patterns.

27. (Unchanged) The system in claim 21, wherein said shaped clock signals include clock signals having a longer than 50% high state duration for the one state data and a shorter than 50% high state duration for the zero state data.

Add claims 28-43 as follows:

-- 28. (New) The system in claim 1, wherein said shaped clock signal encodes the information contained in said data signal.

29. (New) The system in claim 1, wherein said shaped clock signal comprises an asymmetric binary signal component.

30. (New) The system in claim 1, wherein said shaped clock signal comprises a synchronous binary signal component.

31. (New) The system in claim 1, wherein said shaped clock signal comprises an asynchronous binary signal component.

32. (New) The system in claim 1, wherein said shaped clock signal comprises one or both of a synchronous and asynchronous multi-level signal component.

33. (New) The system in claim 1, wherein said shaped clock signal is selected from the group of signal types consisting of: an aysmmetric binary signal, a synchronous binary signal, an asynchronous binary signal, a synchronous multi-level signal, an asynchronous multi-level signal, and combinations thereof.

34. (New) The system in claim 1, wherein said data information encoded within said clock shaped signal is processed by a processor which includes one or more of clock signal modulation and clock signal shaping processing component.

35. (New) The system in claim 1, wherein said processing of said clock shaped signal comprises processing selected from the group consisting of signal transmission, signal receiving, signal modulation, signal demodulation, asynchronous or synchronous binary modulation, asynchronous or synchronous multi-level modulation including modulation of three or more levels,

36. (New) The system in claim 1, wherein said clock shaped signals include Clocked Shaped (CS) signals or Clock Modulated (CM) signals.

37. (New) The system in claim 1, wherein said clock shaped signal comprises a Clock Modulated (CM) signal including an asymmetrical clock signal having different clock signal shapes wherein the data information to be transmitted by the clock shaped signal is contained in one or more of the shapes of the clock signals and/or in the differences of the clock signal shapes.

38. (New) The system in claim 1, wherein said shaped clock signals include shaped clock modulated signals.

39. (New) The system in claim 1, wherein said data information is communicated using signal shaping of asymmetrical and/or of symmetrical clock signaling elements rather than of signal shaping of symmetrical data signaling elements.

40. (New) The system in claim 1, wherein said shaped clock signals have been shaped and filtered to reduce the spectrum required to communicate the information encoded in the clock.

41. (New) The system in claim 1, wherein said data information is encoded in non-symmetric and asynchronous clock signals.

42. (New) The system in claim 1, wherein said non-symmetric and asynchronous clock signals encode the data information with means other than time-clock edge transitions, specific clock durations, or specific clock positions.

43. (New) A method of signaling comprising:

selecting a shaped data information bearing clock signal from a plurality of shaped data information bearing clock signals including shaped clock signals having at least one first shaped clock having a longer duration relative to a second shaped clock and said second shaped clock having a shorter duration relative to said first shaped clock, said shaped data information bearing clock signals being selected from the group of signals consisting of: shaped symmetrical data information bearing clock signals, shaped non-symmetrical data information bearing clock signals, two-level non-symmetrical data information bearing

clock signals, multilevel non-symmetrical data information bearing clock signals, variable rise and different non-symmetrical fall time data information bearing clock signals, asynchronous data information bearing clock signal information, and combinations thereof;

cross-correlating said selected shaped clock signal;

quadrature modulating said cross-correlated shaped clock signal;

demodulating said received shaped clock signal; and

decoding said received demodulated shaped clock signal to regenerate said selected shaped data information bearing clock signal.--

REMARKS

This Preliminary Amendment is submitted pursuant to Rule 115, and no new matter has been introduced. Entry of the Amendment is respectfully requested. Claims 1, 4-9, and 11-43 are pending after entry of the amendment.

Respectfully Submitted,
FLEHR HOHBACH TEST ALBRITTON & HERBERT LLP

By _____
R. Michael Ananian
Reg. No. 35,050

Four Embarcadero Center #3400
San Francisco, CA 94111
(650) 494-8700

1018422